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Aijia Yao
aijia@mit.edu

Design-technology Co-optimization of 2D Electronics
A. Yao, J. Zhu, T. Palacios
Sponsorship: SRC Jump 2.0 SUPREME Center

With 2D electronics becoming more mature in both material synthesis and device integration technologies, Design-Technology Co-optimization (DTCO) has been used in designing complex electronic devices based on 2D materials and optimizing device performance and material properties. However, there still lacks an efficient electrical characterization method to provide real-time evaluation and accurate feedback for every process step from material growth to device fabrication. Meanwhile, it is also critical to conduct compact, accurate device modeling especially for high-performance transistors with scaled channel length.

In this project, we investigated fast electrical characterization methods based on circular transmission line model (CTLM) structures. We developed a parameterized cell(PCell) to aid CTLM layout design and fabricated global back-gated devices with both transferred and direct-grown 2D thin films. The convenience of only one lithography step allows seamless testing of different combinations of dielectric materials, metal contacts and passivation layers. The samples were examined by scanning electron microscope (SEM) and contour detection algorithms were used to identify the fabrication-induced variation, domain size, effective channel length and width. These data offered experimental calibration for precise device modeling, which later contributed to design and performance predictions based on TCAD simulation. Simulation models were further studied focusing on highly-scaled transistors with channel length below 10 nm. We expect this fabrication, characterization and modeling pipeline to ultimately facilitate future DTCO processes with improved efficiency and accuracy for novel materials and devices.

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Ayush Sagar Gupta

ayushg@mit.edu

Ohmic Contacts to Ultrawide-Bandgap Two-Dimensional Semiconductors
A. S. Gupta, J. Zhu, T. Palacios
Sponsorship: Army Research Office (ARO)

Power transistors for fast switching high voltage applications require wide bandgaps to enable large breakdown fields. Silicon carbide (SiC) and gallium nitride (GaN) thus offer advantages over silicon for high-voltage devices and circuits. However, these materials still have limited bandgaps (~3.5 eV) and are difficult to integrate with circuits based on other material systems. The emerging ultrawide-bandgap (UWBG) two-dimensional (2D) semiconductors, which have bandgaps above 5 eV, are expected to provide even better performance thanks to their wider bandgaps, higher critical fields, and atomic thinness. However, forming ohmic contacts to UWBG 2D materials such as hexagonal boron nitride (h-BN) and 2D GaN is very challenging due to their extreme band misalignment with metal contacts, difficulties in realizing substitutional doping, and the Fermi level pinning effect.

Here, we investigate potential approaches to forming ohmic contacts to UWBG 2D semiconductors. Modulation doping can be used to introduce more carriers to the transistor channel without significantly deteriorating carrier mobility. Dipole moments, graded 2D heterostructures, and highly-doped UWBG oxides, are all investigated to tune both the contact metal work function and the band edge of UWBG semiconductors. A combination of these techniques can be used to form ohmic contacts to UWBG 2D materials, thus enabling the next generation of power electronic devices with higher operation voltage as well as future integrated circuits with increased functionalities.

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Christian Lopez Angeles

chris_la@mit.edu

Highly integrated graphene-based sensing platform for structural monitoring applications

Christian Lopez Angeles, Tomas Palacios

Sponsorship: Ferrovial

Two-dimensional materials, such as graphene, hold promise for sensing applications. Graphene's remarkable surface-to-volume ratio, when employed as a transducer, enables the sensor channel to be readily modulated in response to chemical changes in proximity to its surface, effectively converting chemical signals into the electrical domain. However, the adoption of this material in sensors has been constrained due to variations in device-to-device performance arising from synthesis and fabrication processes.

To address this challenge, here we used arrays of tens of Graphene Field Effect Transistors (GFETs) to develop a robust and multiplexed chemical sensing system. This array is coupled with custom-designed high-speed readout electronics for structural monitoring applications.

As an initial application, we focused on the monitoring of reinforced concrete structures. Under harsh environmental conditions, structures constructed from reinforced concrete may experience degradation due to corrosion, a chemical process initiated by carbonation of the concrete layer and significant fluctuations in temperature and humidity. Under normal conditions, concrete maintains a pH level within the alkaline range of 13 to 14. However, when subjected to carbonation, its pH decreases to values between 8 and 9.

Our platform has demonstrated real-time pH monitoring of reinforced concrete structures. By conducting I-V sweep measurements in the sensor channel, we have established a correlation between [H+] concentration and the gate-source voltage (Vgs) at graphene's Dirac point with an accuracy of roughly 98%. This system and correlation allow for the prompt detection of any deviations induced by corrosion within a concrete environment.

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Deniz Erus

dierus@mit.edu

Thermal Management in GaN High Electron Mobility Transistors (HEMT)

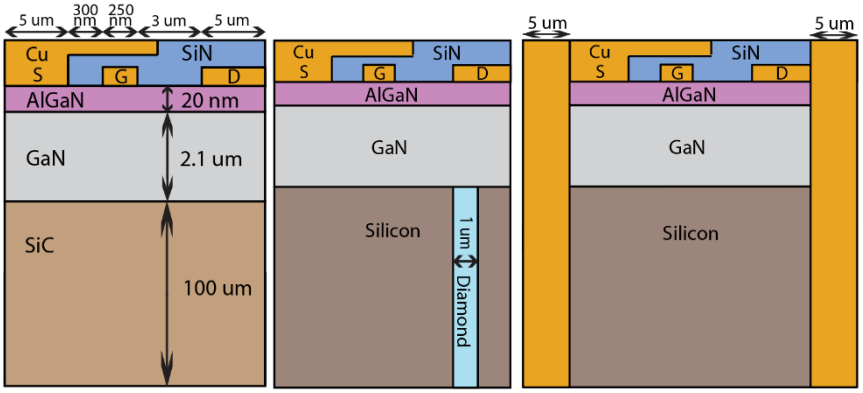
D. Erus, T. Palacios

Wide bandgap and large breakdown voltage of GaN make GaN high electron mobility transistors (HEMTs) a key building block for the next generation of high-power and high-frequency electronics. However, the large power density in these devices induces harsh and localized self-heating in their conducting channel.

GaN-on-Si structures enables the use of state-of-the-art fabrication tools which reduces defects and increases the yield. Yet, due to the lower thermal conductivity of Si substrates compared to SiC, GaN-on-Si HEMT has a higher peak temperature than the commonly used GaN-on-SiC at the same power dissipation level.

In this work, the same Silvaco TCAD simulation framework and transistor geometry are used to find thermal solutions that decrease the peak temperature of GaN-on-Si HEMT to a comparable value with GaN-on-SiC. This is achieved by making a 1-μm-diamond-via under the drain (38% decrease in R_{th}). When the sides of the GaN-on-Si HEMT is covered with Cu, it reaches a lower peak temperature than GaN-on-SiC (70% decrease in R_{th}).

(a) GaN-on-SiC HEMT structure; (b) GaN-on-Si HEMT with 1 um diamond via; (c) GaN-on-Si HEMT with copper covered sides.



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Ezekiel Daye
egdaye@mit.edu

High Temperature RF GaN electronics.
J. Niroula, Q. Xie, T. Palacios
Sponsorship: Sponsorship: AFOSR (Grant No. FA9550-22-1-0367)

High temperature rated electronics are needed for many emerging applications including hypersonic aircrafts, deep well oil drilling, and exploration of Venus. However, traditional Si devices cannot operate beyond 250°C which is significantly below the typical temperature range required for these applications. Wide-band semiconductors such as SiC and GaN are well suited for high temperature operation because of their wide-band gap and negligible carrier thermal generation at these temperatures (around 500°C). In spite of offering significant advantages in a wider range of applications from power and RF to MEMS and digital circuits, their use in high temperature analog and digital circuits remains relatively unexplored. In this project, we have developed a robust experimental characterization and modeling framework for the characterization and simulation of AlGaN/GaN High Electron Mobility Transistor (HEMT) devices across a wide temperature range from 25°C to 500°C. The project involved the following subtasks: 1) Development of automated analysis code based on automatic DC-IV measurements that show device performance metrics across entire sample area; 2) Development of automated model extraction routine based on DC-IV measurements; and 3) physics simulations of device in TCAD software to estimate projected performance based on changes in device design.

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Gillian K. Micale

gkmicale@mit.edu

Advanced Materials issues of GaN-on-Si Transistors for RF and Beyond

G.K. Micale, J.A. Perozek, Q. Xie, J. Niroula, H. Pal, P. Yadav, P.C. Shih, and T. Palacios

Sponsorship: SRC Jump 2.0 SUPREME Center

In an age of ever-increasing demand for high-speed communications and wireless technology, gallium nitride high-electron-mobility-transistors (GaN HEMTs) have emerged as a breakthrough technology to meet the frequency and power demands of modern electronics. Owing to their large breakdown voltages and high electron saturation velocity, GaN high electron mobility transistors (HEMTs) are the leading technology for power and RF applications. Using Si substrates for GaN heteroepitaxy would dramatically increase the cost-efficiency of GaN RF devices, but due to the lattice mismatch and low resistivity and thermal conductivity of Si substrates, GaN-on-Si device performance has lagged SiC, the leading substrate choice for high-frequency GaN devices. Achieving a deeper understanding of parasitics and their causes will enable major improvements to cutoff frequency (f_T) and maximum oscillation frequency (f_{max}) and offer helpful insights for fabricating more advanced device architectures.

Low resistance regrown ohmic contacts will help increase f_{max}. Combining reactive ion etching with novel wet etching techniques during contact fabrication is an effective way to control the sidewall angle and mitigate plasma damage in the recessed GaN, which will improve the regrown GaN/2DEG channel interface and reduce the contact resistance. In this work, we study two wet etching methods to use with ICP dry etching to optimize the interfaces of GaN recesses: (1) KOH and (2) a Digital Etch (DE) that alternates between H_2SO_4/H_2O_2 and dilute HCl.

Both etching methods preferentially etch semi-polar faces of GaN but have different impacts on the sidewall angle. Comparing contact resistance from devices made with each method will help deconvolve the impact of plasma damage and sidewall angle on contact resistance. Furthermore, investigating the role of plasma damage, topology, and interface impurities on channel carrier density and contact resistivity that will facilitate ultralow resistance ohmic contacts that will play a key role in future high-power, high-frequency HEMT architectures.

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Hae Won Lee
hw93528@mit.edu

Novel tellurium contacts for p-type WSe_2 devices
H. W. Lee, J. Zhu, K. Reidy, F. Ross, J. Kong and T. Palacios
Sponsorship: Intel (ISRA)

Since the first discovery of graphene[1], extensive research on two-dimensional (2D) semiconductors has opened promising possibilities for elevating 2D semiconductor applications from the academic to the industrial level for the next generation of electronics. Now, 2D semiconductors can be grown at a large scale[2], processed using Si CMOS-compatible fabrication techniques, and demonstrate high-performance transistors with low contact resistance[3]. However, these remarkable improvements have mainly been achieved with n-type 2D semiconductors, primarily focusing on molybdenum disulfide (MoS_2). In the case of p-type 2D semiconductors, such as tungsten diselenide (WSe_2), there are still significant challenges in material growth and reducing contact resistance to make them comparable to n-type 2D transistors. These challenges hinder the demonstration of 2D complementary metal-oxide-semiconductor (CMOS) circuits at an industrial level. In particular, reducing the contact resistance between a p-type 2D channel and a metal contact is essential to achieving high-performance p-type transistors.

In this work, we explore the use of semimetal tellurium (Te) as contacts for p-type WSe_2 transistors. Semimetals such as bismuth (Bi) and antimony (Sb) are known to mitigate the Fermi level pinning effect at the interface between the metal and MoS_2, thereby drastically reducing the contact resistance of MoS_2 transistors[4]. We compare the performance of WSe_2 transistors with various contact materials, including Te, palladium (Pd), and platinum (Pt), and observe that Te contacts indeed reduce the Fermi level pinning effect at the interface of WSe_2 and Te. In addition, we enhance the performance of WSe_2 transistors by adjusting the deposition temperature of Te. This research on semimetal Te contacts will serve as an important baseline study for novel contacts for p-type 2D transistors.

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John Niroula
jniroula@mit.edu

High Temperature RF GaN Electronics
E. Daye, J. Niroula, Q. Xie, T. Palacios
Sponsorship: Sponsorship: AFOSR (Grant No. FA9550-22-1-0367)

High temperature electronics has received much interest recently due to emerging applications in geothermal well exploration, hypersonic flight electronics, and space exploration. GaN based devices are an exciting contender for extremely high temperature environments due to their high mobility, high saturation velocity, especially beyond 250°C, which is the limit of traditional silicon-based devices. In this project we aim to develop a high performing GaN based RF devices that operates at both room temperature as well as 500°C, by developing highly scaled, high temperature refractory tungsten T-gates with AlN gate dielectric (Figure 1 below) that has record current density at 500°C. Such high temperature ready devices will allow high performing RF communication systems operating
in the extreme conditions needed to enable the aforementioned applications.

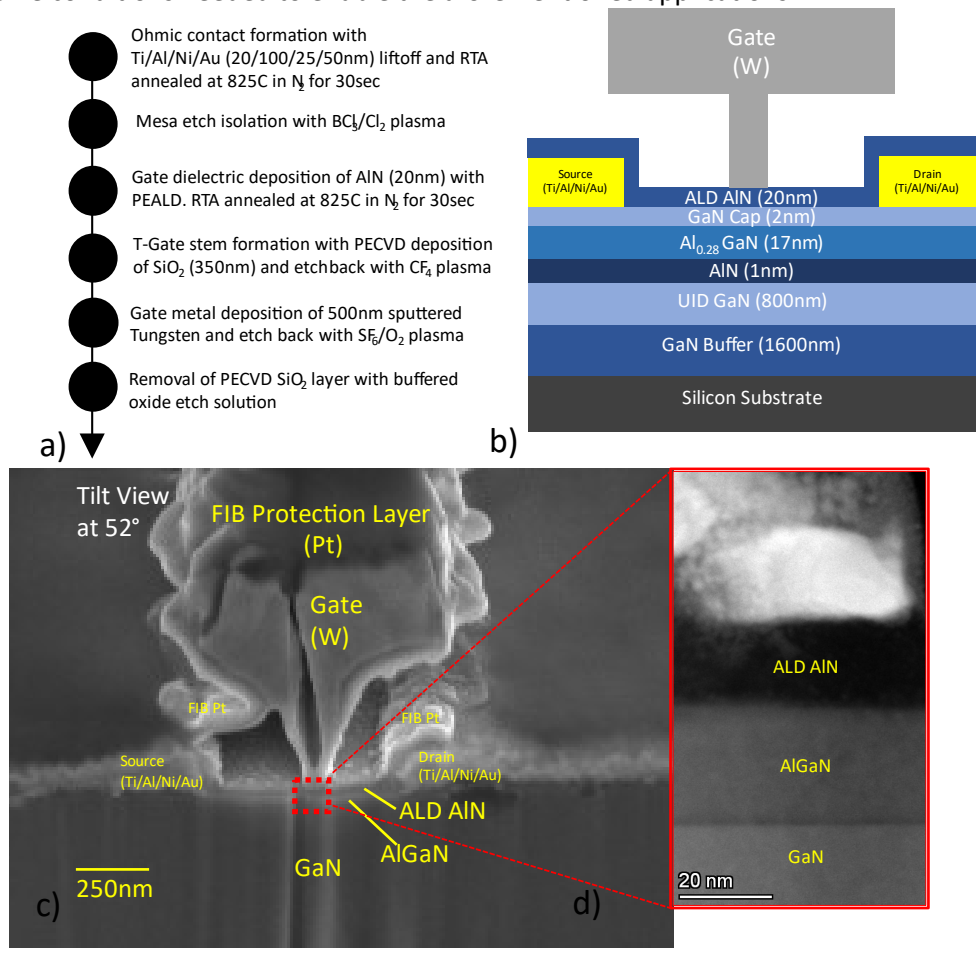

Figure 1. a) Device fabrication process flow b) Cartoon schematic of device structure c) Fabricated device SEM cross section d) TEM view of inset shown in c)

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Jung-Han (Sharon) Hsia

jhsia@mit.edu

First Demonstration of Optically Controlled Vertical GaN Power finFETs
J.-H. Hsia, J. Perozek and T. Palacios
Sponsorship: Office of Naval Research (Grant No. N00014-22-1-2468)

In recent years, the boost in consumer electronics and data centers has increased the electricity demand. The delivery and transformation of power though electric grids require many efficient power converters and electronics that can withstand high current and voltages. However, traditional power electronics are mostly electrically triggered, which can complicate the circuitry design and cause electromagnetic interference (EMI). The use of optically triggered devices will simplify the circuitry design, reduce EMI and potentially increase the operating frequency. In this work, we have demonstrated, for the first time, an optically-controlled vertical GaN transistor with J_{DS} > 90A/cm^2 at V_{DS} = 3V under an illumination intensity of 1μW, which translates into an optical responsivity > 10^5 A/W. The initial results have demonstrated potential of these devices for future high-power electronics.

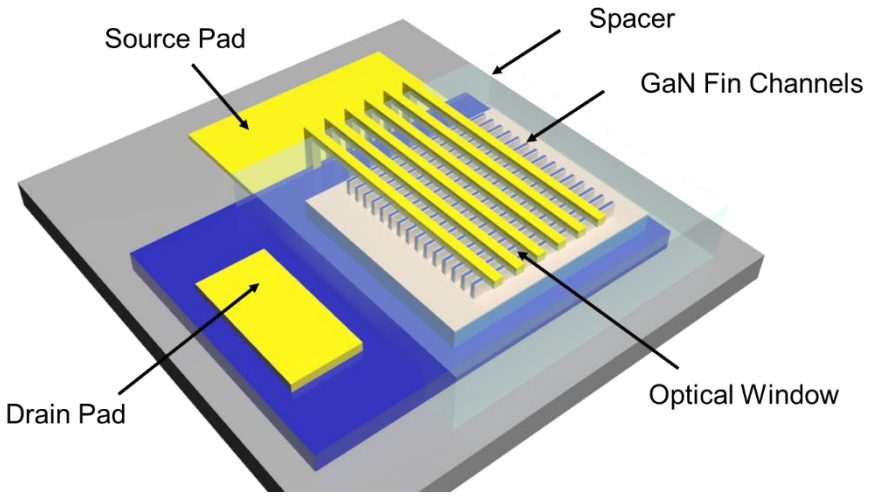

Figure 1. Device schematic of an optically-controlled vertical GaN finFET.

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Miguel Grande Raez

miguel24@mit.edu

Chamber and airflow optimization for E-Nose Technology

M. Grande, C. Lopez Angeles, T. Palacios

Sponsorship: Universidad Politecnica de Madrid (UPM)

Electronic nose (E-nose) technology has been explored for years. However, it has not yet achieved the digitization of the sense of smell. Various concepts of E-noses have been proposed, but none presents a practical solution for complex environments, often yielding non-reproducible results. In this context, we are designing an E-nose system based on FET sensors employing two-dimensional materials such as graphene and MoS_2. Each sensor chip is equipped with a thousand sensing units, aiming for enhanced robustness in measurements.

These sensors, integrated with a PCB system and an external computer, will enable the detection of biomarkers in exhaled breath. To optimize the performance, these devices are housed in an engineered-designed chamber, ensuring efficient airflow for detection. Furthermore, simulations of airflow with finite element modeling method will be utilized to enhance sensing module performance. The air samples can be obtained either by exhaling into the chamber or by activating a vacuum extraction pump to capture ambient air. Additionally, the study explores the characterization of the sensors using essential oils, which can provide valuable insights into biomarker detection. This research represents a significant step toward achieving a practical E-nose system for diverse applications, including disease diagnosis and environmental monitoring.

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Minsik Oh
oms9585@mit.edu

A Comprehensive Study on Si-ion Implanted Ohmic Contacts on AlGaN/GaN Heterostructure
M. Oh, Q. Xie, and T. Palacios
Sponsorship: "Advanced Research Projects Agency-Energy (ARPA-E) (grant no. DE-AR0001591)

Ohmic contacts to III-Nitride heterostructures pose challenges due to the wide band gap and the limitations of existing methods, e.g. low throughput for MBE regrown contacts, rough surface morphology for alloyed contacts, and the use of metal stacks that are incompatible with Si fabs. In contrast, implanted contacts offer ease of manufacturing with precise doping control and uniformity.

This work delves into Si-ion implanted ohmic contacts on AlGaN/GaN heterostructures. The contact resistance (R_C) of the implanted contacts can be divided in three components: R_{c1}, the resistance between the metal and the implanted region; R_{c2}, the resistance of the implanted region; and R_{c3}, the resistance between the implanted region and the two-dimensional electron gas (2DEG). R_{c1} reached a minimum when the ohmic metals were deposited after etching the entire AlGaN layer. R_{c2} is proportional to the length of the implanted region between the metals and 2DEG, thus can be reduced through precise lithography, such as electron beam lithography. R_{c3} was reduced by employing a dual-path implantation technique that increased the Si concentration at the interface between the implanted region and 2DEG. Both R_{c1} and R_{c2} had minimum values with a middle dose, indicating that a higher dose would lead to an increase in both carrier density and lattice damage, making the optimum value lie in the middle range.

Moreover, this work explores, for the first time, high-temperature Si-ion implantation to form ohmic contacts on AlGaN/GaN heterostructures. Room temperature, 300 °C, and 500 °C were explored in this work, and XRD results demonstrated that less lattice damage was created by the implantation at high temperature. Electrical characterization showed that the higher the implant temperature, the more carriers were activated, resulting in lower R_{c1} and R_{c2} values. Consequently, the lowest R_c (average: 0.20 Ω·mm, minimum 0.14 Ω·mm) was obtained from 500 °C implantation with a dose of 3×10^{15} cm^{-2}.

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Patrick Darmawi-Iskandar
pdi@mit.edu

Next-Generation High-Performance GaN Complementary Technology
P. K. Darmawi-Iskandar, Q. Xie, J. Niroula, T. Palacios
Sponsorship: Samsung Electronics Co., Ltd. (033517-00001), Qualcomm Inc. (MAS-492857), and National Defense Science and Engineering Graduate Fellowship

n-FET based GaN ICs have offered record levels of efficiency, power, and compactness for data centers, power adapters, electric vehicles (EVs), and 5G/6G telecommunication systems. A GaN complementary (GaN-CMOS) technology seeks to offer fundamental performance improvement in both efficiency and density of power electronics. Over the years, significant research has been conducted on GaN-CMOS at MIT and worldwide, including material epitaxy, transistor architectures and process optimization. However, the scaling limits of GaN CMOS for lower voltage applications have not been fully explored and understood.

This work seeks to explore the low voltage scaling limits of enhancement-mode n-channel p-GaN-gate HEMTs, through the combination of the following approaches: (1) material epitaxy, especially the polarization-inducing barrier; (2) novel transistor architecture to ensure good gate control at short channels; (3) improved processing to achieve aggressive scaling in these transistors.

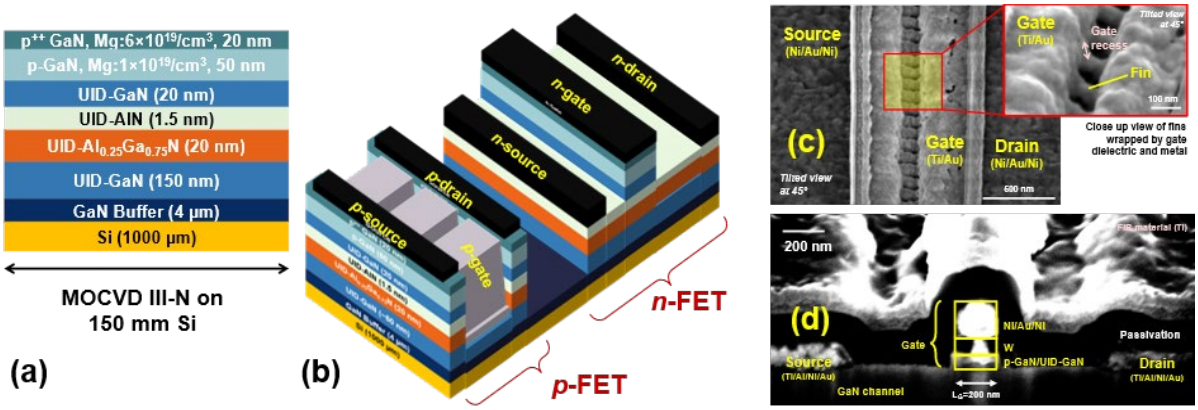

Figure: Highly scaled GaN complementary technology (CT). (a) Epitaxial structure. (b) Device structures of p-FET (SA FinFET) and n-FET (SA-gate p-GaN-gate HEMT) based on the same GaN-on-Si platform as illustrated in Fig. 1(a). (c), (d) Scanning electron microscopy (SEM) images of representative p-FET and n-FET, respectively.

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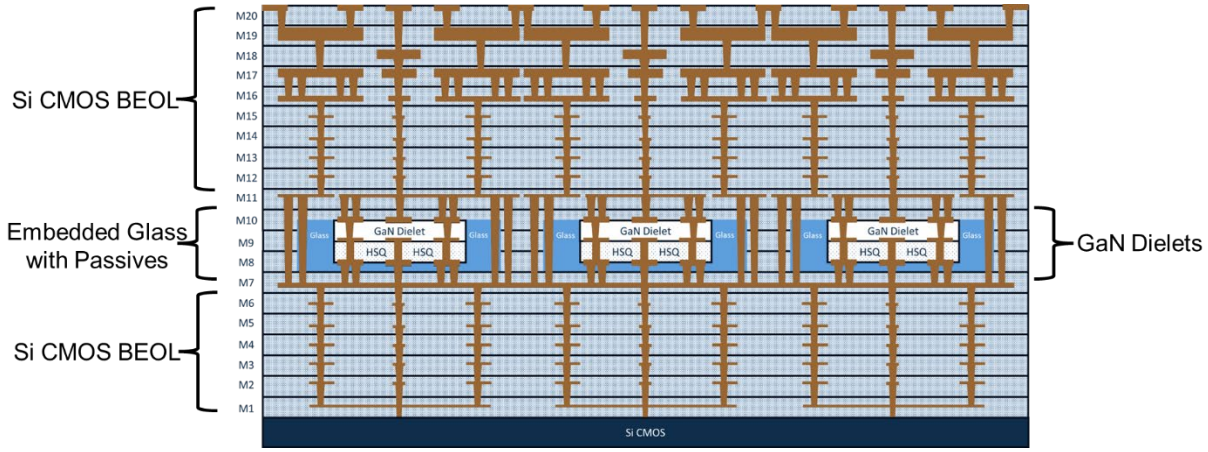
Pradyot Yadav
yadavps@mit.edu

Development of a GaN and Si CMOS Stacked-3DIC Platform for W-G Band Applications
P. Yadav, J. Niroula, Q. Xie, T. Palacios
Sponsorship: AFOSR (Grant no. FA9550-22-1-0367) , SRC JUMP 2.0 (Grant no. 2023-JU-3136), Lockheed Martin Corp. (Grant no. 025570-00036), and ARPA-E (Grant no. DE-AR0001591), and the National Defense and Science Graduate Fellowship

With data rates pushing into the Tbps for AR/VR, there is an urgent need for the use of sub-terahertz RF front ends and transistors. Gallium Nitride (GaN) transistors are an ideal candidate for the front-end-of-line (FEOL) as they push the limits of high-power density, high frequency semiconductor devices. Furthermore, silicon is a preferred option for the back-end-of-line (BEOL) due to ease of manufacturing and access to complementary logic technology for digital circuits.

In this system, 3D-stacked GaN dielets, connected via highly-scaled interconnects in the Si BEOL, will be optimally placed to ensure uniform and minimal thermal degradation in the system. CTE-matched glass will also be embedded in the silicon to allow for passive fabrication. This approach will yield a bespoke chip design, tailor-made for the given high-speed application.

To design the most efficient high data rate communication systems, we also explore the use of a design/system-technology co-optimization (DTCO/STCO) approach, that combines innovative GaN dielets with state-of-the-art Silicon (Si) bias and control circuitry, and passives in glass via advanced heterogeneous integration.



(a) Single chip 3DIC with multiple GaN dielets leveraging Si BEOL and embedded glass for passives

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Yixuan Jiao
yjiao917@mit.edu

Low temperature wafer-scale synthesis of 2D TMD material for Back-end-of-line Heterogeneous Integration
Y. Jiao, J. Zhu, T. Palacios
Sponsorship: Center for Heterogeneous Integration of Micro Electronic Systems (JUMP 2.0)

Two-dimensional (2D) transition metal dichalcogenide (TMD) materials have demonstrated promising future in the next generation of highly scaled microelectronic devices for their excellent electronic and photonic properties such as high mobility, direct bandgap in combination with their atomic scale dimensions. These properties have also made 2D TMD materials ideal candidate for back-end-of-line (BEOL) integration with silicon front-end integrated circuits (IC). However, the current method of transfer integration of 2D TMD material and Si IC potentially introduces damages and defects to the material, thus greatly impedes the performance of fabricated devices. Direct growth of TMD was traditionally proven difficult in BEOL process due to temperature limits (<400°C).

In this work, we explore the low temperature large wafer-scale direct synthesis of high quality 2D TMD (MoS_2, $MoTe_2$, WSe_2, etc.) which are BEOL compatible. The MOCVD system we designed is capable of direct growth on platforms up to 200 mm in diameter. The BEOL compatibility is achieved through separation of high temperature precursor decomposition region and low temperature deposition region. This enables monolayer TMD materials direct integration with Si front end devices without introducing damage, thus maintaining the optimal device performance. This integration technique shall bring a promising future of heterogeneous integration of TMD with various front-end substrates and applications in flexible electronics, optoelectronics and other monolithic 3D integration electronics.

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